encountered in non-linear DAC are solved.

While the invention has been shown typical preferred embodiments of the invention, it should be apparent to those skilled in the art that is not so limited but is susceptible to various changes without departing from the scope of the invention. For instance, the PWM, in the present invention, is used to modulate 5 bits data, and DAC is used to convert 3 bits data, but PWM can be used to modulate 4 bits data and DAC is used to convert 4 bits data.

What is claimed is :

1. A driving method of speaker for converting digital sound data into corresponding driving signals to drive said speaker, comprising the steps of:

dividing said digital sound data into two groups, first data group and second data group;

modulating said first data group into driving signals represented by pulse width; and

converting said second data group into driving signals represented by pulse height.

2. A driving method as set forth in Claim 1, wherein said first data group is higher bits data group and said second data group is lower bits data group.

3. A driving method as set forth in Claim 1, wherein said first data group is higher bits data group and said second data group is lower bits data group.

4. A driving circuit of speaker for converting digital sound data into corresponding driving signals to drive said speaker, said digital sound data being divided into a higher bits data group and a lower bits data group, which circuit comprising:

a pulse width modulation circuit being used to modulate said higher bits data group into driving signals represented by pulse width; and

a pulse height conversion circuit being used to convert said lower bits data group into driving signals represented by pulse height.

5. A driving circuit of speaker as set forth in Claim 4, wherein the pulse width modulation circuit comprises:

a counter;

an accumulator having one input terminal connected to said higher bits data group;

a first comparator for comparing the output of said counter with the output of said accumulator;

a second comparator for comparing the output of the counter with the higher bits data group; and

a XOR gate having two input terminals being connected to the outputs of said first comparator and the second comparator, respectively.

6. A driving circuit of speaker as set forth in Claim 5, wherein the counter starts counting from 0 at the beginning of every sound sampling cycle.

7. A driving circuit of speaker as set forth in Claim 5, wherein the output of the first comparator is HI when the counting value of said counter is smaller than the output value of said accumulator.

8. A driving circuit of speaker as set forth in Claim 7, wherein the output of the second comparator is HI when the counting value of said counter is smaller than the output value of said higher bit group.

9. A driving circuit of speaker as set forth in Claim 4, wherein the pulse height conversion circuit comprises:

a plurality of AND gates, one input terminal of each said AND gates being commonly connected to the output of said XOR gate, and the other input terminal of said AND gates being respectively connected to the lower bits data group; and

a plurality of current sources with different current ratio controlled by the output of said AND gates and the output of the second comparator, the output of said current sources being commonly connected to said speaker.

10. A driving circuit of speaker for converting digital sound data into corresponding driving signals to drive said speaker, said digital sound data being divided into a

higher bits data group and a lower bits data group, comprising:

a pulse heigh conversion circuit being used to convert said higher bits data group into driving signals represented by pulse height; and

a pulse width circuit being used to convert said lower bits data group into driving signals represented by pulse width.

11. A driving circuit of speaker as set forth in Claim 10, wherein the pulse width modulation circuit comprises:

a counter; and

a comparator for comparing the output of said counter with the value of said lower bits data group.

12. A driving circuit of speaker as set forth in Claim 11, wherein the counter starts counting from 0 at the beginning of every sound sampling cycle.

13. A driving circuit of speaker as set forth in Claim 12, wherein the output of the first comparator is HI when the output value of the counter is smaller than the output value of the accumulator.

14. A driving circuit of speaker as set forth in Claim 13, wherein the pulse height modulation circuit comprises:

an accumulator having an input terminal connected to the higher bits data group;

a multiplexer having an input terminal connected to the higher bits data group and the output of the accumulator, a selection terminal being connected to the output of the comparator; and

a plurality of current sources with different current ratio being respectively controlled by the output of said multiplexer, and the output of said current sources being commonly connected to said speaker.

15. A driving circuit of speaker as set forth in Claim 14, wherein when the selection terminal of the multiplexer is HI, the output of said accumulator is selected as the

output of said multiplexer.

16. A driving circuit of speaker as set forth in Claim 14, wherein the selection terminal of the multiplexer is LOW, the higher bits data group is selected as the output of said multiplexer.